Refine Search

Search Results -

Terms	Documents
(backplane near5 (card or board)) same switch$3 same ((hot or live) adj1 (plug$4 or swap$4))	25

Database:
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Search: L1

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Search History

DATE: Friday, February 18, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L1	(backplane near5 (card or board)) same switch$3 same ((hot or live) adj1 (plug$4 or swap$4))	25	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
(backplane near5 (card or board)) same switch$3 same ((hot or live) adj1 (plug$4 or swap$4))	1

Database:
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US Patents Full-Text Database
US OCR Full-Text Database
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Search: L2

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Friday, February 18, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L2	(backplane near5 (card or board)) same switch$3 same ((hot or live) adj1 (plug$4 or swap$4))	1	L2
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L1	(backplane near5 (card or board)) same switch$3 same ((hot or live) adj1 (plug$4 or swap$4))	25	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
(439/92 |361/695 |361/720 |361/752 |361/683 |361/687 |709/222 |709/227 |709/219 |709/203 |709/223 |710/301 |710/302 |710/72 |710/304 |363/123 |713/100).ccls.	21440

Database:
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Search: L3

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Friday, February 18, 2005 Printable Copy Create Case

Set Name	Query
side by side	
	DB=PGPB,USPT,USOC; PLUR=YES; OP=OR
L3	710/301,302,72,304;713/100;709/222,227,219,203,223;361/695,720,752,683,687;363/123;439/9
	DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR
L2	(backplane near5 (card or board)) same switch$3 same ((hot or live) adj1 (plug$4 or swap$4))
	DB=PGPB,USPT,USOC; PLUR=YES; OP=OR
L1	(backplane near5 (card or board)) same switch$3 same ((hot or live) adj1 (plug$4 or swap$4))

END OF SEARCH HISTORY

h e b b cg b e e ch

Refine Search

Search Results -

Terms	Documents
L1 and L3	8

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L4

Refine Search

Recall Text | Clear | Interrupt

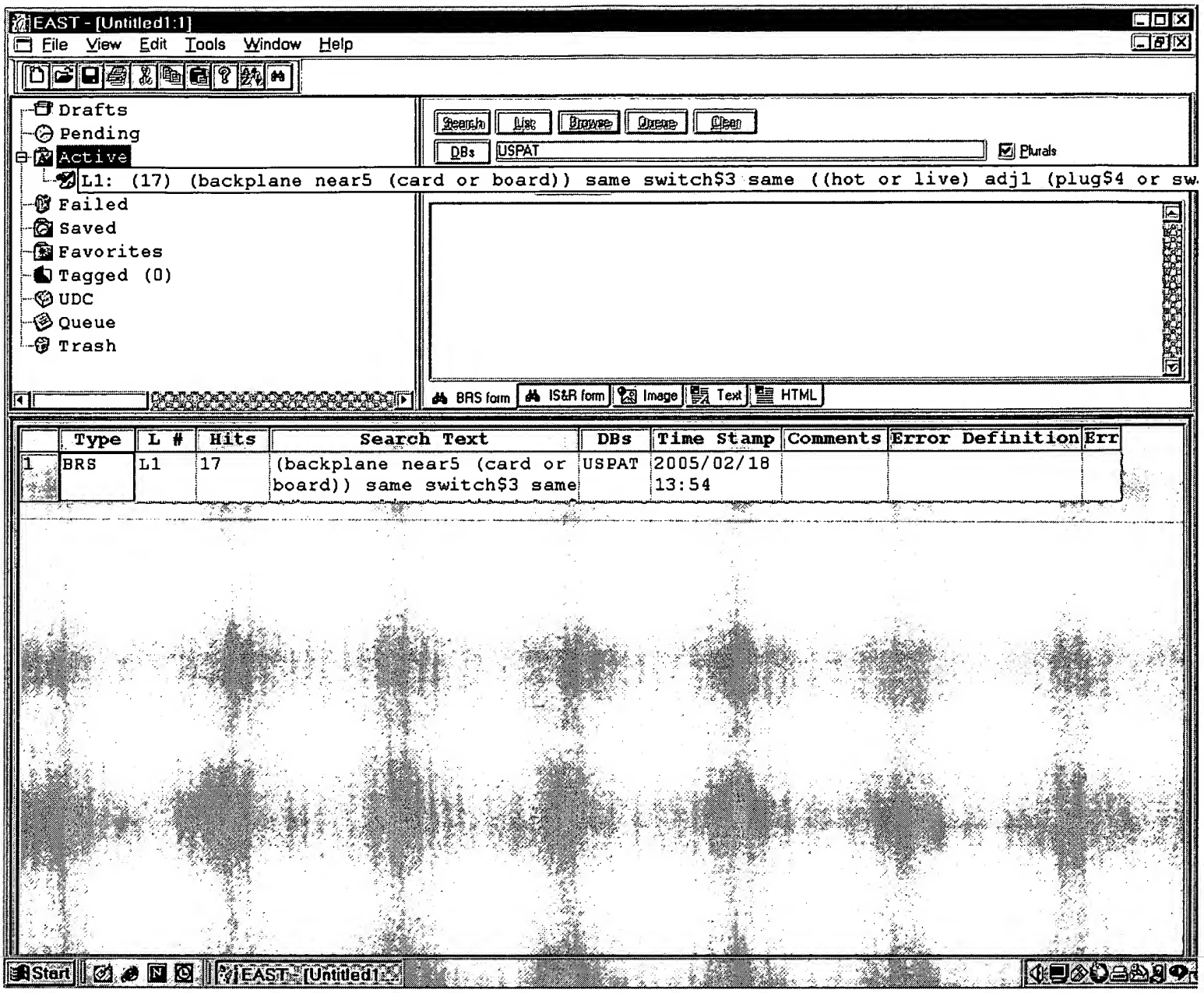
Search History

DATE: Friday, February 18, 2005 Printable Copy Create Case

Set Name side by side	Query
	DB=PGPB,USPT,USOC; PLUR=YES; OP=OR
L4	l1 and L3
L3	710/301,302,72,304;713/100;709/222,227,219,203,223;361/695,720,752,683,687;363/123;439/9
	DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR
L2	(backplane near5 (card or board)) same switch$3 same ((hot or live) adj1 (plug$4 or swap$4))
	DB=PGPB,USPT,USOC; PLUR=YES; OP=OR
L1	(backplane near5 (card or board)) same switch$3 same ((hot or live) adj1 (plug$4 or swap$4))

END OF SEARCH HISTORY

h e b b cg b e e ch


EAST - [Untitled1:1]
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Drafts
Pending
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L1: (17) (backplane near5 (card or board)) same switch$3 same ((hot or live) adj1 (plug$4 or sw
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1 BRS L1 17 (backplane near5 (card or board)) same switch$3 same USPAT 2005/02/18 13:54
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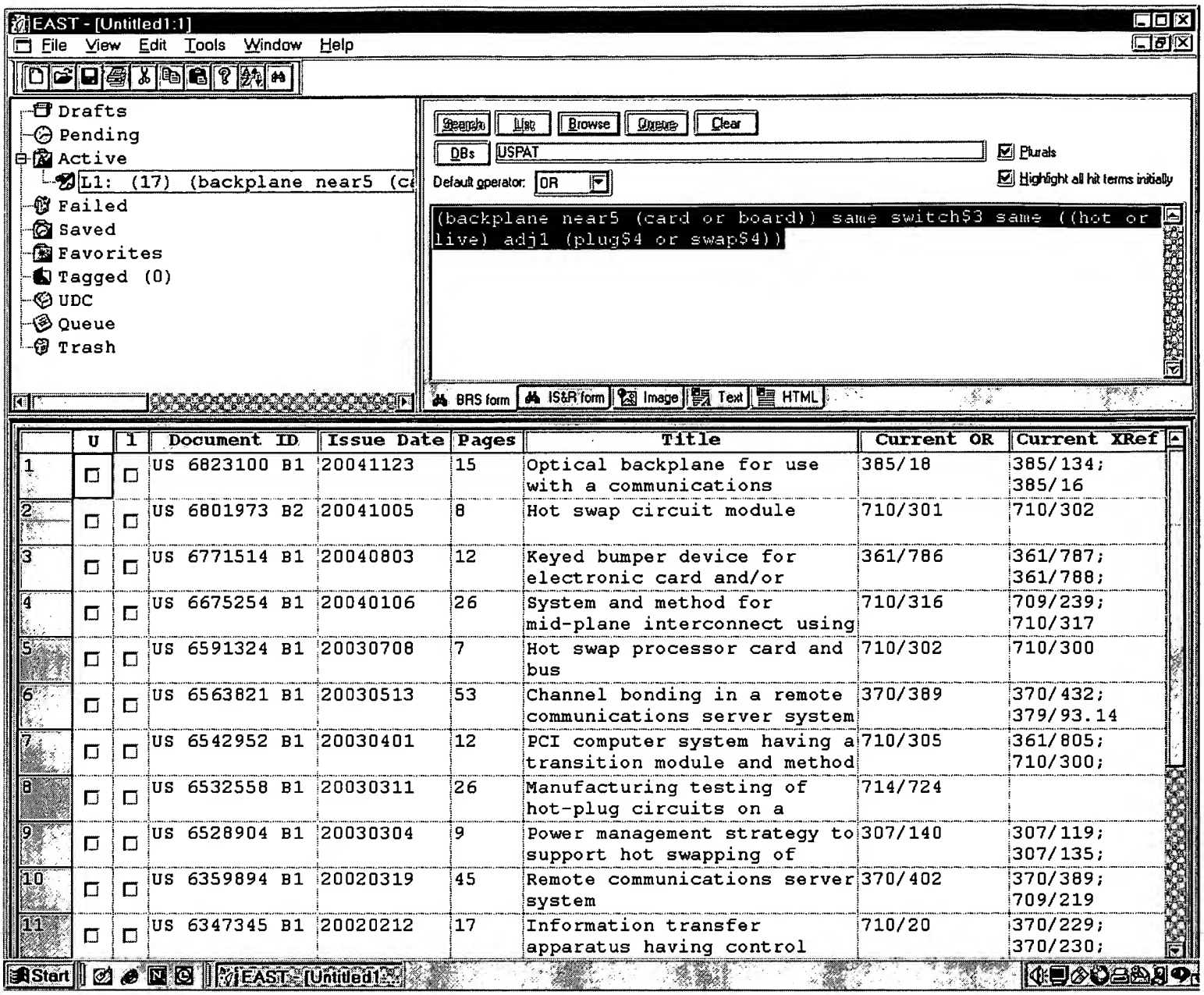

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	☐	☐	US 6823100 B1	20041123	15	Optical backplane for use with a communications	385/18	385/134; 385/16
2	☐	☐	US 6801973 B2	20041005	8	Hot swap circuit module	710/301	710/302
3	☐	☐	US 6771514 B1	20040803	12	Keyed bumper device for electronic card and/or	361/786	361/787; 361/788;
4	☐	☐	US 6675254 B1	20040106	26	System and method for mid-plane interconnect using	710/316	709/239; 710/317
5	☐	☐	US 6591324 B1	20030708	7	Hot swap processor card and bus	710/302	710/300
6	☐	☐	US 6563821 B1	20030513	53	Channel bonding in a remote communications server system	370/389	370/432; 379/93.14
7	☐	☐	US 6542952 B1	20030401	12	PCI computer system having a transition module and method	710/305	361/805; 710/300;
8	☐	☐	US 6532558 B1	20030311	26	Manufacturing testing of hot-plug circuits on a	714/724	
9	☐	☐	US 6528904 B1	20030304	9	Power management strategy to support hot swapping of	307/140	307/119; 307/135;
10	☐	☐	US 6359894 B1	20020319	45	Remote communications server system	370/402	370/389; 709/219
11	☐	☐	US 6347345 B1	20020212	17	Information transfer apparatus having control	710/20	370/229; 370/230;

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backplane and (card or board) and (plug* or swap*) Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

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1 **BIST circuit design for backplane interconnect test**
Chang, J.-K.;
Science and Technology, 1999. KORUS '99. Proceedings. The Third Russian-K International Symposium on , Volume: 2 , 22-25 June 1999
Pages:685 - 688 vol.2

[Abstract] [PDF Full-Text (340 KB)] **IEEE CNF**

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2 **IEEE standard for a metric equipment practice for microcomputers convection-cooled with 2.5mm connectors**

IEEE Std 1301.3-1992 , 2 April 1993
[Abstract] [PDF Full-Text (388 KB)] **IEEE STD**

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3 **IEEE standard for a metric equipment practice for microcomputers convection-cooled with 2 mm connectors**

IEEE Std 1301.1-1991 , 9 Jan. 1992
[Abstract] [PDF Full-Text (1028 KB)] **IEEE STD**

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4 **High speed EPICS data acquisition and processing on one VME boar**
Merl, R.; Gallegos, F.; Pillai, C.; Shelley, F.; Sanchez, B.J.; Steck, A.;
Particle Accelerator Conference, 2003. PAC 2003. Proceedings of the , Volume 4 , 12-16 May 2003
Pages:2518 - 2520 vol.4

[Abstract] [PDF Full-Text (1377 KB)] **IEEE CNF**

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5 **622 Mbit/s board-to-board link in 0.5 µm CMOS technology**
Gogaert, S.; Steyeart, M.; Peluso, V.;

Custom Integrated Circuits Conference, 1995., Proceedings of the IEEE 1995 , May 1995
Pages:447 - 450

[Abstract] [PDF Full-Text (372 KB)] IEEE CNF

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6 **Electrical two and three dimensional modelling of high-speed board board interconnections**
Gailus, M.; Fusi, M.A.; Zanella, F.;
WESCON/'95. Conference record. 'Microelectronics Communications Technolo Producing Quality Products Mobile and Portable Power Emerging Technologies' Nov. 1995
Pages:100

[Abstract] [PDF Full-Text (288 KB)] IEEE CNF

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7 **A new distributed real-time controller for robotics applications**
Buhler, M.; Whitcomb, L.; Levin, F.; Koditschek, D.E.;
COMPCON Spring '89. Thirty-Fourth IEEE Computer Society International Conference: Intellectual Leverage, Digest of Papers. , 27 Feb.-3 March 1989
Pages:63 - 69

[Abstract] [PDF Full-Text (652 KB)] IEEE CNF

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8 **IEEE standard for mechanical core specifications for microcomputer using IEC 60603-2 connectors**

IEEE Std 1101.1-1998 , 18 Dec. 1998
[Abstract] [PDF Full-Text (1452 KB)] IEEE STD

---

9 **IEEE standard for mechanical core specifications for microcomputer using IEC 603-2 connectors**

IEEE Std 1101.1-1991 , 18 June 1992
[Abstract] [PDF Full-Text (1688 KB)] IEEE STD

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10 **IEEE standard for mechanical core specifications for microcompute**

ANSI/IEEE Std 1101-1987 , 29 April 1988
[Abstract] [PDF Full-Text (1416 KB)] IEEE STD

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11 **A plug and play approach to data acquisition**
Toledo, J.; Muller, H.; Buytaert, J.; Bal, F.; David, A.; Guirao, A.; Mora, F.J.;
Nuclear Science, IEEE Transactions on , Volume: 49 , Issue: 3 , June 2002
Pages:1190 - 1194

[Abstract] [PDF Full-Text (219 KB)] IEEE JNL

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12 **A plug&play approach to data acquisition**
Toledo, J.; Muller, H.; Buytaert, J.; Bal, F.; David, A.; Guirao, A.; Mora, F.J.;
Nuclear Science Symposium Conference Record, 2001 IEEE , Volume: 1 , 4-1(Nov. 2001
Pages:506 - 510 vol.1

[Abstract] [PDF Full-Text (1138 KB)] **IEEE CNF**

13 **Bonded Gold Fingers as a Low-Cost Alternative to Patterned Edgeb Fingers for General PWB use**
Brown, V.;
Components, Hybrids, and Manufacturing Technology, IEEE Transactions on [s also IEEE Trans. on Components, Packaging, and Manufacturing Technology, I A, B, C] , Volume: 1 , Issue: 3 , Sep 1978
Pages:274 - 281

[Abstract] [PDF Full-Text (1424 KB)] **IEEE JNL**

14 **The LANL Neutron-Science-Center time-of-flight/position-sensitive detect module: status and progress**
Rose, C.R.; Hammonds, J.P.; Nelson, R.A.; Weizeorick, J.T.;
Nuclear Science, IEEE Transactions on , Volume: 47 , Issue: 2 , April 2000
Pages:151 - 153

[Abstract] [PDF Full-Text (152 KB)] **IEEE JNL**

15 **Signal switching in automated test system for the transfer function characterization**
Manuel, A.; Roset, X.; Gomez, J.; Garrido, A.; Carlosena, A.; Romos, R.;
Instrumentation and Measurement Technology Conference, 1999. IMTC/99. Proceedings of the 16th IEEE , Volume: 2 , 24-26 May 1999
Pages:1206 - 1210 vol.2

[Abstract] [PDF Full-Text (672 KB)] **IEEE CNF**

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A plug&play approach to data acquisition

Toledo, J. Muller, H. Buytaert, J. Bal, F. David, A. Guirao, A. Mora, F.J.
Dept. of Electron. Eng., Univ. Politecnica de Valencia, Spain

This paper appears in: **Nuclear Science Symposium Conference Record,**

Publication Date: 4-10 Nov. 2001
On page(s): 506 - 510 vol.1
Volume: 1
ISSN: 1082-3654
Number of Pages: 4 vol. l+2518
Inspec Accession Number: 7329273

Abstract:
Backplane buses are becoming a legacy for high rate, high volume data proc applications. Higher efficiency at lower cost is offered by the PCI bus technolo compared to crate-embedded processors. Becoming part of the **plug**&play do host's operating system, no additional data transfer protocols are needed. We combined the PCI technology with high-density FPGA logic and common mezz standards on a flexible PCI **card**. First applications cover readout controllers f bus protocols, high-speed link I/O and fast analog input data conversion. A fie programmable gate array (FPGA) with embedded PCI master/target core serv programmable interface between the PCI bus, mezzanine **cards** and a local S Adapter mezzanine **cards**, implemented according to the IEEE P1386 or simil standards, are used for level conversion, trigger interfacing or preprocessing. application-dependent controller functions as well as SDRAM and PCI interfaci handled by FPGA logic. A Linux driver was developed to achieve high bandwid initiated transfers. Control software for Windows and an interface for LabView control and monitoring applications via graphical interfaces. First experience a applications will be reported.

Index Terms:
PLD programming application specific integrated circuits data acquisition device dri programmable gate arrays graphical user interfaces high energy physics instrumenta computing nuclear electronics operating systems (computers) physical instrumentat readout electronics system buses trigger circuits IEEE P1386 LabView target cont driver PCI bus technology SDRAM Windows application-dependent controller func **backplane** buses common mezzanine standards control software crate-embedded data acquisition fast analog input data conversion field programmable gate array gr

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interfaces high rate high volume data processing high-density FPGA logic high-spe
operating system plug&play approach programmable interface readout controllers
trigger interfacing used for level conversion

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L1: Entry 2 of 25 File: PGPB Oct 30, 2003

PGPUB-DOCUMENT-NUMBER: 20030204658
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030204658 A1

TITLE: Hot swap circuit module

PUBLICATION-DATE: October 30, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Wu, Chung-Kai	Taoyuan Hsien		TW	

APPL-NO: 10/ 128229 [PALM]
DATE FILED: April 24, 2002

INT-CL: [07] H05 K 7/10, G06 F 13/00

US-CL-PUBLISHED: 710/302
US-CL-CURRENT: 710/302

REPRESENTATIVE-FIGURES: 4

ABSTRACT:

A hot swap circuit module for a switch system having a backplane. The module includes a circuit board and a latch circuit. The circuit board has a plurality of pins for inserting into the backplane.

The latch, disposed on the circuit board, has a data input terminal for receiving an important signal, and a control terminal for receiving a clock signal to latch the important signal.

The latch circuit is utilized to eliminate malfunction resulting from the disturbance voltage caused by hot swapping. Any circuit with latch function is allowed to be applied to the switch system of the present invention such that the switch system operates more stably without special pins or additional bus controller.

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L1: Entry 8 of 25 File: PGPB Jun 20, 2002

PGPUB-DOCUMENT-NUMBER: 20020078290
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020078290 A1

TITLE: Cluster computer network appliance

PUBLICATION-DATE: June 20, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Derrico, Joel Brian	Atlanta	GA	US	
Freet, Paul Jonathan	Duluth	GA	US	

APPL-NO: 09/ 987917 [PALM]
DATE FILED: November 16, 2001

RELATED-US-APPL-DATA:
Application is a non-provisional-of-provisional application 60/248834, filed November 16, 2000,

INT-CL: [07] G06 F 13/00

US-CL-PUBLISHED: 710/302
US-CL-CURRENT: 710/302

REPRESENTATIVE-FIGURES: 1

ABSTRACT:

A method of mounting a hot-swappable module in a computer network appliance, the module comprising a hot swap connector including ground pins, power pins and signal pins, the computer network appliance including a backplane board having hot swap mating connectors, the method comprising connecting the ground pins of the hot swap connector of the module with corresponding ground elements of a hot swap mating connector of the backplane board; connecting the power pins of the hot swap connector of the module with corresponding power elements of the hot swap mating connector of the backplane board after the ground pins have made contact; and connecting the signal pins of the hot swap connector of the module with corresponding signal elements of the hot swap mating connector of the backplane board after the power pins have made contact. The computer network appliance further comprises a hot-swappable CPU module, a hot-swappable power module, and a hot-swappable ethernet switch module. Each of the CPU module, power module and ethernet switch module includes a hot swap connector for connecting with a specific hot swap mating connector of the backplane board. The CPU module operates as a stand alone computer. The CPU module comprises hardware BIOS for configuring the CPU module and instructing a network attached storage (NAS) to locate an operating system (OS) from which to boot. The CPU module is configured to boot remotely from

an OS located in the NAS without user intervention. The remote booting ability of the CPU module allows the CPU module to run different types of operating systems without the need for a local hard disk drive (HDD), which increases the mean time between failure (MTBF) and decreases the mean time to repair (MTTR) of the computer network appliance.

[0001] This application claims priority from U.S. Provisional Application Serial No. 60/248,834, filed Nov. 16, 2000. The entirety of that provisional application is incorporated herein by reference.

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L1: Entry 25 of 25 File: USPT Jun 25, 1996

US-PAT-NO: 5530302
DOCUMENT-IDENTIFIER: US 5530302 A

TITLE: Circuit module with hot-swap control circuitry

DATE-ISSUED: June 25, 1996

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Hamre; John D.	Plymouth	MN		
Wicklund; Denton G.	Delano	MN		
Barkley; Steven D.	Roseville	MN		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Network Systems Corporation	Minneapolis	MN			02

APPL-NO: 08/ 180623 [PALM]
DATE FILED: January 13, 1994

INT-CL: [06] H01 J 13/00

US-CL-ISSUED: 307/147; 395/280
US-CL-CURRENT: 307/147; 710/100

FIELD-OF-SEARCH: 395/325, 395/750, 395/800, 395/500, 361/58, 361/100, 361/118, 361/62, 439/377, 307/147

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	3993935	November 1976	Phillips et al.	361/748
☐	4700348	October 1987	Ise et al.	371/8.2
☐	4750136	May 1988	Arpin et al.	364/514B
☐	4835737	May 1989	Herrig et al.	395/325
☐	4999787	March 1991	McNally et al.	364/514B
	5272584	December 1993	Austruy et al.	361/58

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☐				
☐	5277615	January 1994	Hastings et al.	439/377
☐	5317697	May 1994	Husak et al.	395/325

OTHER PUBLICATIONS

EDN-Product Update--dated Nov. 12, 1992.
Electronic Engineering Times article dated Jul. 20, 1992.

ART-UNIT: 217

PRIMARY-EXAMINER: Shoop, Jr.; William M.

ASSISTANT-EXAMINER: Kaplan; Jonathan S.

ATTY-AGENT-FIRM: Haugen and Nikolai

ABSTRACT:

A circuit board capable of live-insertion or hot-swapping into a live chassis backplane. The circuit board is provided with a power control circuitry for gracefully ramping up board power after insertion, or gracefully removing power just prior to physical removal of a circuit board from the board slot. A pair of ejector levers are provided on each side of the circuit board. A push button switch is provided proximate one ear thereof and is selectively opened or closed depending upon the position of an ejector cover which can be secured thereover in an interlocking relationship. Upon retraction of the extractor cover, the switch is opened, and the converse applies. Power MOSFETs are provided between the card edge and the board power busses which are gracefully turned on and off as a function of the switch position. A high-side gate driver provides an increased bias voltage, which bias voltage is communicated through the closed switch to the gates of the MOSFETs. An RC network is coupled to the MOSFET gate to determine the time constant at which bias voltage will be ramped up or ramped down to correspondingly ramp power up or down to the circuit board power busses. A power supply monitor circuit is also provided for automatically resetting the board upon a power up condition.

16 Claims, 8 Drawing figures

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Search Results - Record(s) 1 through 8 of 8 returned.

☐ 1. Document ID: US 20030204658 A1

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L4: Entry 1 of 8 File: PGPB Oct 30, 2003

PGPUB-DOCUMENT-NUMBER: 20030204658
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030204658 A1

TITLE: Hot swap circuit module

PUBLICATION-DATE: October 30, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Wu, Chung-Kai	Taoyuan Hsien		TW	

US-CL-CURRENT: 710/302

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWMC | Draw De

☐ 2. Document ID: US 20020078290 A1

L4: Entry 2 of 8 File: PGPB Jun 20, 2002

PGPUB-DOCUMENT-NUMBER: 20020078290
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020078290 A1

TITLE: Cluster computer network appliance

PUBLICATION-DATE: June 20, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Derrico, Joel Brian	Atlanta	GA	US	
Freet, Paul Jonathan	Duluth	GA	US	

US-CL-CURRENT: 710/302

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWMC | Draw De

h e b b g e e e f e ef b e

☐ 3. Document ID: US 6801973 B2

L4: Entry 3 of 8 File: USPT Oct 5, 2004

US-PAT-NO: 6801973
DOCUMENT-IDENTIFIER: US 6801973 B2

TITLE: Hot swap circuit module

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWMC | Draw. De

☐ 4. Document ID: US 6591324 B1

L4: Entry 4 of 8 File: USPT Jul 8, 2003

US-PAT-NO: 6591324
DOCUMENT-IDENTIFIER: US 6591324 B1

TITLE: Hot swap processor card and bus

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWMC | Draw. De

☐ 5. Document ID: US 6359894 B1

L4: Entry 5 of 8 File: USPT Mar 19, 2002

US-PAT-NO: 6359894
DOCUMENT-IDENTIFIER: US 6359894 B1

TITLE: Remote communications server system

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWMC | Draw. De

☐ 6. Document ID: US 6212586 B1

L4: Entry 6 of 8 File: USPT Apr 3, 2001

US-PAT-NO: 6212586
DOCUMENT-IDENTIFIER: US 6212586 B1

TITLE: Hot-swappable high speed point-to-point interface

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWMC | Draw. De

☐ 7. Document ID: US 6091609 A

L4: Entry 7 of 8 File: USPT Jul 18, 2000

US-PAT-NO: 6091609

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DOCUMENT-IDENTIFIER: US 6091609 A

TITLE: Electronic circuit card having transient-tolerant distribution planes

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWMC | Draw De

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☐ 8. Document ID: US 6032209 A

L4: Entry 8 of 8 File: USPT Feb 29, 2000

US-PAT-NO: 6032209
DOCUMENT-IDENTIFIER: US 6032209 A

TITLE: Hot-swappable high speed point-to-point interface

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWMC | Draw De

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Terms	Documents
L1 and L3	8

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US006801973B2

(12) **United States Patent**
Wu

(10) **Patent No.: US 6,801,973 B2**
(45) **Date of Patent: Oct. 5, 2004**

(54) **HOT SWAP CIRCUIT MODULE**

(75) Inventor: Chung-Kai Wu, Taoyuan Hsien (TW)

(73) Assignee: Accton Technology Corporation, Hsinchu (TW)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 387 days.

(21) Appl. No.: 10/128,229

(22) Filed: Apr. 24, 2002

(65) Prior Publication Data

US 2003/0204658 A1 Oct. 30, 2003

(51) Int. Cl.[7] G06F 13/00
(52) U.S. Cl. 710/301; 710/302
(58) Field of Search 710/100, 300, 710/301, 302, 303, 304; 361/18, 58; 307/147

(56) References Cited

U.S. PATENT DOCUMENTS

5,272,584 A * 12/1993 Anstey et al. 361/58
5,530,302 A * 6/1996 Hamre et al. 307/147
5,572,395 A * 11/1996 Ramens et al. 361/58
5,787,261 A * 7/1998 Osaka et al. 710/302
5,922,060 A * 7/1999 Goodnum 710/302
6,041,375 A * 3/2000 Bass et al. 710/302

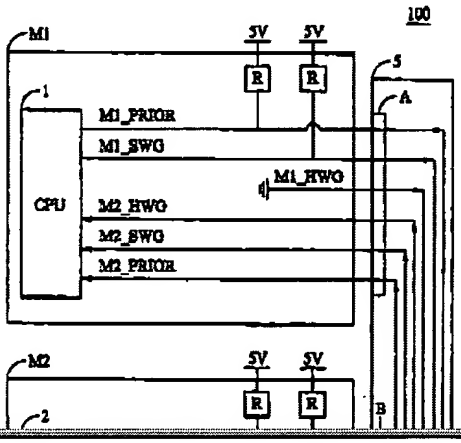
* cited by examiner

Primary Examiner—Khanh Dang
(74) *Attorney, Agent, or Firm*—Birch, Stewart, Kolasch & Birch, LLP

(57) **ABSTRACT**

A hot swap circuit module for a switch system having a backplane. The module includes a circuit board and a latch circuit. The circuit board has a plurality of pins for inserting into the backplane. The latch, disposed on the circuit board, has a data input terminal for receiving an important signal, and a control terminal for receiving a clock signal to latch the important signal. The latch circuit is utilized to eliminate malfunction resulting from the disturbance voltage caused by hot swapping. Any circuit with latch function is allowed to be applied to the switch system of the present invention such that the switch system operates more stably without special pins or additional bus controller.

8 Claims, 4 Drawing Sheets



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(12) **United States Patent**
Allen et al.

(10) **Patent No.: US 6,532,558 B1**
(45) **Date of Patent: Mar. 11, 2003**

(54) **MANUFACTURING TESTING OF HOT-PLUG CIRCUITS ON A COMPUTER BACKPLANE**

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(73) Assignee: **International Business Machines Corporation, Armonk, NY (US)**

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/518,230**

(22) Filed: **Mar. 2, 2000**

(51) **Int. Cl.**[7] **H04B 17/00**
(52) **U.S. Cl.** **714/724**
(58) **Field of Search** 714/724, 46, 22, 714/36; 710/103, 316

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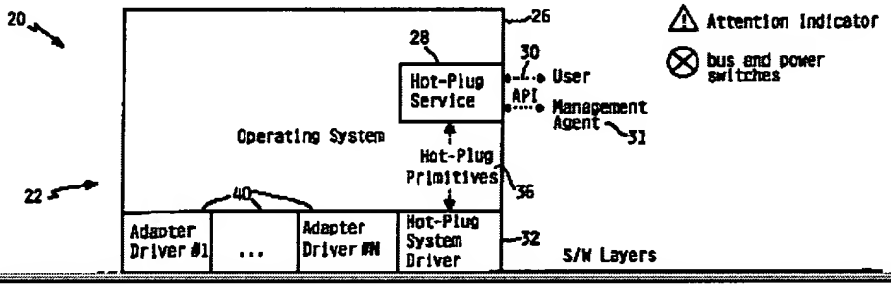
Primary Examiner—Phung M. Chung
(74) *Attorney, Agent, or Firm*—James R. Nock

(57) **ABSTRACT**

A method and apparatus for analog testing of hot-plug circuits on an active computer backplane. A test connector is added to the computer backplane that enables an external tester to turn on each card slot present on the computer backplane. The external tester then directs a test adapter card residing in a selected card slot to apply a nominal and overcurrent load to each voltage level of the selected card slot. After each load has been applied, the corresponding voltage level is returned to the external tester. The external tester then measures the voltage level, and verifies that the voltage level falls within a predefined voltage range. The test connector uses existing unutilized bus signal lines to pass test directives and results between the card slot under test and the external tester. The same test adapter card that performs the analog test on a card slot is also used to perform digital testing on the card, thus reducing both testing time and the complexity of the testing apparatus.

24 Claims, 19 Drawing Sheets



US005530302A

United States Patent [19]

Hamre et al.

[11] Patent Number: 5,530,302

[45] Date of Patent: Jun. 25, 1996

[54] **CIRCUIT MODULE WITH HOT-SWAP CONTROL CIRCUITRY**

[75] Inventors: John D. Hamre, Plymouth; Denton G. Wicklund, Delano; Steven D. Barkley, Roseville, all of Minn.

[73] Assignee: Network Systems Corporation, Minneapolis, Minn.

[21] Appl. No.: 180,623

[22] Filed: Jan. 13, 1994

[51] Int. Cl.[6] H01J 13/00

[52] U.S. Cl. 307/147; 395/280

[58] Field of Search 395/325, 750, 395/800, 500; 361/58, 100, 118, 62; 439/377; 307/147

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Primary Examiner—William M. Shoop, Jr.
Assistant Examiner—Jonathan S. Kaplan
Attorney, Agent, or Firm—Haugen and Nikolai

[57] ABSTRACT

A circuit board capable of live-insertion or hot-swapping into a live chassis backplane. The circuit board is provided with a power control circuitry for gracefully ramping up board power after insertion, or gracefully removing power just prior to physical removal of a circuit board from the board slot. A pair of ejector levers are provided on each side of the circuit board. A push button switch is provided proximate one ear thereof and is selectively opened or closed depending upon the position of an ejector cover which can be secured thereover in an interlocking relationship. Upon retraction of the extractor cover, the switch is opened, and the converse applies. Power MOSFETs are provided between the card edge and the board power busses which are gracefully turned on and off as a function of the switch position. A high-side gate driver provides an increased bias voltage, which bias voltage is communicated through the closed switch to the gates of the MOSFETs. An RC network is coupled to the MOSFET gate to determine the time constant at which bias voltage will be ramped up or ramped down to correspondingly ramp power up or down to the circuit board power busses. A power supply monitor circuit is also provided for automatically resetting the board upon a power up condition.

16 Claims, 6 Drawing Sheets